Design and Generation of High-Performance Transceivers

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In the AI-driven era, high-performance communication circuits must support extremely high data throughput, demanding over 100 Gb/s per channel. To address these challenges, we present two key research items: high-speed transceiver design and automated custom layout generation.

First, we developed a PAM-8 based transceiver architecture capable of transmitting 3 bits per symbol. A carefully engineered multi-path receiver chain ensures robust signal recovery and high fidelity, enabling the highest mixed-signal PAM-8 data rate reported to date. This design addresses both bandwidth and signal integrity challenges inherent in modern AI SoC environments.

Second, we introduce LAYGO, a layout generation framework that leverages a template-and-grid methodology to significantly reduce manual effort and design complexity. The framework has been successfully applied to advanced semiconductor platforms including sub-7nm FinFETs, DRAM, and CMOS image sensors, achieving over 5x productivity improvement. Its modular design supports rapid adaptation to various circuit topologies and design rules.

We are now actively extending this framework through the integration of artificial intelligence and large language models (LLMs), aiming to further automate layout tasks and improve design quality. This research is being conducted in close collaboration with industry partners, ensuring both academic innovation and practical relevance.

References

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